Management of Technical Projects Within OpenHW Group

***draft Framework for Review by TWG***

*Change History*

*1 – Duncan Bees, June 30 - initial analysis of current situation*

* 1. *Duncan Bees, July 1 - added clarifications on concept of vertical projects*
  2. *Duncan Bees, July 7 - clarifications on project descriptions, committers added*

*2.0 Duncan Bees, July 14 - rewritten as a draft project management framework*

*3.0 Duncan Bees July 21 - modify tech milestones*

*4.0 Duncan Bees July 28 - after TWG meeting. describe PL gate milestones in greater detail, add Maintenance Project*

*5.0 Jérôme Quévremont July 29 2020 - review and update*

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*7.0 Duncan Bees rewrite based based on review and Jerry’s comments*

*8.0 Duncan Bees fixed section numbering*

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# **Introduction**

## Scope of this Document

This document describes the organization of the technical activities of the OpenHW Group which lead to published output such as open source artifacts related to hardware and software, and technical specifications. These activities are carried out by OpenHW members and staff.

This document does not address OpenHW activities such as board initiatives, marketing, or internal staff activities.

## Definition of OpenHW Project

The OpenHW projects covered by this document fall in the following categories:

* OpenHW Technical Projects (OTP)
* OpenHW Specification Projects (OSP).

### **OpenHW Technical Projects (OTP)**

During OpenHW Technical Projects (OTP), members develop a technical output. The output is made available to the public according to an open source license. The open source development process used is the Eclipse Development Process (EDP). <https://www.eclipse.org/projects/dev_process/>

A typical OTP comprises one or more of the following deliverables in source code, and possibly object format:

* Integrated circuit design IP (DIP)
* Integrated circuit verification IP (VIP)
* Software
* FPGA IP and FPGA designs
* Board level hardware descriptions such as schematics, Gerber files, and/or Bill Of Materials
* ASIC prototypes possibly with reference design boards

### **OpenHW Specification Projects (OSP).**

During OpenHW Specification Projects (OSP), members develop a technical standard. The process followed is the Eclipse Foundation Specification Process.

<https://www.eclipse.org/projects/efsp/>

Further definition is required for OpenHW OSP project methodology.

### **Project Roles**

#### Technical Project Leader

Each OpenHW project has at least one Technical Project Leader (TPL) appointed at the Project Launch Gate (see Section 1.3.1.1). The Technical Project Leader may also be the Project Manager (PM), defined in Section 1.1.1.2. The TPL can be a member’s employee or an OpenHW staff employee.

A project may have several TPLs when the project spans multiple phases or aspects or involves effort from multiple Task Groups. In this case, the TPLs coordinate among themselves and with the Project Manager to ensure the TPL responsibilties are carried out,

The TPL(s) reponsibilties are:

* To coordinate technical activities such as verification efforts, chip architecture design, RTL coding efforts, software architecture, software coding, and other technical activities or development.
* To work with individual contributors to plan and review contributions.
* To plan and execute technical integration of projects within TGs and across TGs.
* To review and ensure accuracy of technical documentation

#### Project Manager

The Project Manager (PM) may also be a Technical Project Leader (see Section 1.1.1.1). The PM can be a member’s employee or an OpenHW staff employee.

The PM’s responsibilities are:

* To create the project plan and drive its review with the TWG.
* To ensure that project resource requirements are understood and that resources are available.
* To create a project schedule and track and report progress within the TGs and to the TWG.
* To resolve project issues.

## OTP Project Gates and Milestones

OTP control points are gates and milestones that are tracked so that OpenHW members can understand and manage the state of a project.

Control points comprise both OTP Gates and OTP Technical Milestones. OTP Gates, described in Section 1.3.1 are managed by the Technical Working Group (TWG) and are common to all OTPs.

OTP Technical Milestones, described in Section 1.3.2, are normally tracked at the Task Group (TG) level. As milestones are reached, progress is reported to the TWG. The set of OTP Technical Milestones to be tracked are tailored to each particular project and they are set out in the project plan.

### **Project Gates for OTP**

Project gates for OpenHW Technical Projects are used by the TWG to track projects throughout the proposal development, engineering development, and project closure phases. The flow of a project from initial project proposal to project complete is show in Figure 1

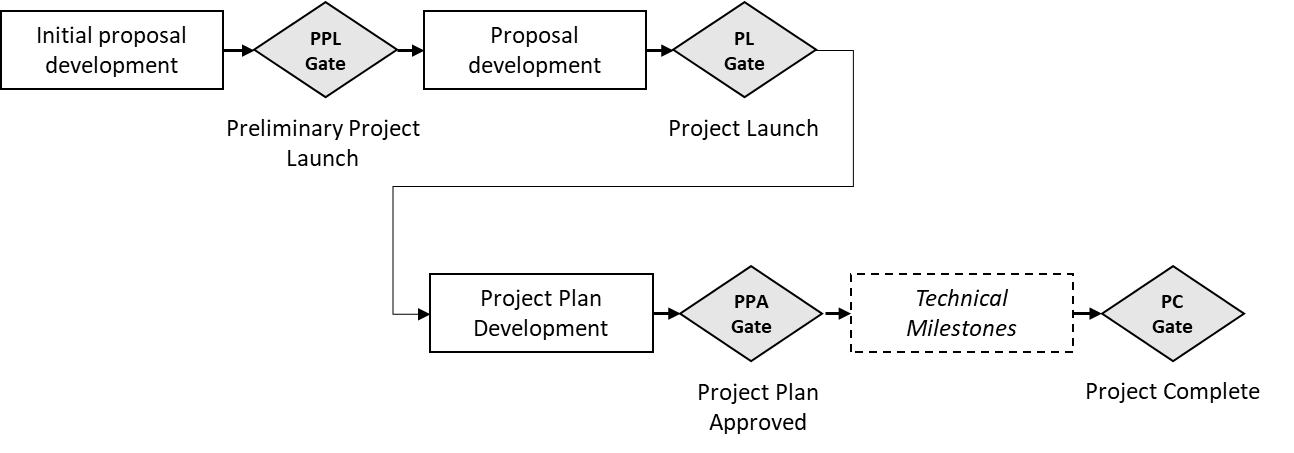


Figure 1 OTP Project Gates

The project gates are summarized in Table 1 below.

|  |  |  |
| --- | --- | --- |
| **Gate** | **Gate Criteria** | **Activities Leading up to Gate** |
| Preliminary Project Launch (PPL) | * Preliminary project proposal meets checklist * TWG majority vote to move forward with project proposal | * OTP pre-proposal development |
| Project Launch (PL) | * PPL gate is already attained. * TWG can hold PPL and PL gate review simultaneously if initial proposal meets both checklists. * PL checklist meets requirements. * TWG majority vote to proceed with project | * OTP proposal development |
| Project Plan Approved (PPA) | * Project plan including schedule and technical milestones has been accepted by TWG majority vote * TWG can hold PL and PPA gate review simultaneously if all required information is available at the PL gate. | * Project plan development |
| Project Complete | * Project deliverables and documentation as set out in project plan are complete * TWG majority vote to complete the project * A maintenance project, if required, has been identified and will be brought forward to TWG for review | * Completion of project work * Identification and scoping any required maintenance project |

Table 1 OTP Project Gates

To avoid unnecessary meetings, the TWG can decide

* to approve PPL and PL gates at the same meeting if all required information is available
* to approve PL and PPA gates at the same meeting if all required information is available.

Note, however, that normally all three gates (PPL, PL, and PPA) are NOT expected to be held simultaneously). The point of multiple gates is to allow projects to be shaped by TWG members who can give early feedback to project proponents at the gate reviews.

### **Basis for TWG Project Gate Decisions**

TWG decisions on launching projects are the key project decisions made by the collective OpenHW membership. OpenHW TWG members are expected to make gate decisions and project recommendations on sound technical perspectives and consideration of the interests of the OpenHW ecosystem.

### **Detailed Project Gate Descriptions**

#### *Project Launch Gates (PPL and PL)*

For a project to be launched, the TWG must review and accept project information prepared by the project proponents concering the project’s technical scope and way of proceeding. The launch gates ensure that project selection criteria determined by the OpenHW community are met prior to project launch.

By granting the Preliminary Project Launch (PPL) Gate, the TWG conveys that OpenHW is potentially interested in undertaking the project subject to further development and review of the proposal at the subsequnet Project Launch (PL) gate. The PPL Gate discussion may identify gaps in the initial proposal that can be filled prior to PL Gate review.

By granting the Project Launch (PL) Gate, the TWG conveys that it accepts the project proposal and the project is launched based on the presented information.

If all the criteria for both PPL and PL are met, the TWG can decide to grant both milestones simultaneously.

|  |  |  |
| --- | --- | --- |
| **Criterion:** | **Preliminary Project Launch (PPL)** | **Project Launch (PL)** |
| Summary of project | preliminary | detailed |
| OpenHW Members committed to participate in project | at least 1 | A substantial set of OpenHW members are interested in participating in/contributing to the proposed project. Typically, at least 3 members commit resources to drive design, verification, review, documentation, and other project activities. The level of participation needed will be established by the TWG taking iaccount the OpenHW mission and the particular nature of the project. |
| Technical Project Leader(s) | (\*)proposed | The identify of Technical Project Leader(s) (described in Section 1.1.1.1) is confirmed. |
| Project Manager | (\*)proposed | The identify of the Project Manager (described in Section 1.1.1.2) is confirmed. Often, the Project Manager is one of the Technical Project Leaders. |
| Summary of requirements (e.g. from assessment of market requirements) | preliminary | Requirements assessment is available with enough detail to provide a well-founded view of project. |
| Explanation of why OpenHW should do this project | preliminary | Explanation of fit between the project and OpenHW community goals, and why OpenHW is well placed to do take on the project. |
| Industry landscape: description of competing, alternative, or related efforts in the industry | preliminary | Industry landscape documented sufficiently to provide explanation of the role that OpenHW project will play in technology development and adoption by taking on this project. |
| List of project outputs | preliminary | All project outputs identified |
| TGs Impacted/Resource requirements | (\*)preliminary | List of TG that will be involved in the technical work with approximate resource requirement per TG, aligning with preliminary resource estimates |
| OpenHW engineering staff resource plan: requirement and availability | (\*)preliminary | OpenHW engineering resource estimated requirements, with availability identified and agreed by OpenHW CEO. |
| Engineering resource supplied by members - requirement and availability | (\*)preliminary | Member engineering resource estimated requirements, with availability identified and agreed by identified members. |
| OpenHW marketing resource - requirement and availability | (\*)preliminary | (\*)OpenHW marketing resource estimated requirements and availability identified and agreed by OpenHW CEO. |
| Marketing resource supplied by members - requirement and availability | (\*)preliminary | (\*)Member marketing resource estimated requirements, with availability identified and agreed by identified members. |
| Funding supplied by OpenHW - requirement and availability | (\*)preliminary | Any specific required funding from OpenHW identified and approved by OpenHW CEO |
| Funding supplied by members - requirement and availability | (\*)preliminary | Any specific required funding from members identified and agreed by identified members |
| External dependencies | (\*)preliminary | Major assumptions regarding required external to OpenHW input, knowledge, tools, cooperation, review, etc. |
| Architecture diagram | (\*)preliminary | (\*)A diagram is available to show the technical architecture of the major components of the project. The diagram may be deferred by decision of the TWG. |
| Who would make use of OpenHW output | preliminary | A description of the typical users of the project output, such as SoC developers, software developers, end users, etc. The description should explain who the primary customers are driving the project requirements. |
| Project license model | preliminary | Description of the licenses under which the project will be released and under which contributions will be made. Compliance of the project license model with terms of the OpenHW Membership Agreement will be verified. |
| Description of initial code contribution, if required | preliminary | A description of the provenance, ownership and content of the initial code contribution, and the license under which it will be contributed. |
| Project distribution model | (\*)preliminary | Description of how and where the project outputs will be distributed. |
| Project plan | (\*)preliminary | preliminary  (note, a completed and detailed project plan is not necessarily required for PL. A further gate, Project Plan Approved is defined in Section 1.3.1.2) |

Table 2 Project Approval Gate Details

(\*) denotes optional criteria for the gate. TWG members can vote to pass a gate if some criteria are incomplete or missing.

#### *Project Plan Approved Gate (PPA)*

The Project Plan Approved (PPA) Gate is a checkpoint indicating that a full project plan is available and has been approved by the TWG.

It is expected that much of the project plan can be directly taken from the PL Gate review materials.

The PL and PPA Gates can be held in a joint meeting if all the required information is available at the PL gate review.

The following table shows the typical elements in the project plan. Note that by approval from the TWG, the Project Manager may modify this list so that an appropriate set of elements is determined for a particular project.

|  |  |
| --- | --- |
| **Project Plan Element** | **Description** |
| Technical Project Leader(s) | As described in Section 1.1.1.1 |
| Project Manager | As described in Section 1.1.1.2 |
| Scope | Overall project scope |
| Project Outputs | The set of project deliverables |
| Work Breakdown | A set of tasks to achieve the project outputs |
| Schedule Baseline | A first-cut view of the project schedule. |
| Design methodology (waterfall, agile, other). | How the work will be organized and planned, for example use of Sprints. |
| Phases | A description of the different releases or phases of the project, if any. |
| Resource Breakdown including key personnel | Resources and their availability, including from OpenHW staff, member companies or other sources. As described in PL gate, or more detailed if required. |
| Tools required | Requirements for tooling, software, etc. |
| Funding resources | Description of how the project and its resources will be funded. |
| Technical milestones to be tracked in project | The list of Technical Milestones and the criteria and process to pass them |
| Project Artifacts | The documents or technical artifacts produced by the project (including the project outputs and those not intended as outputs). |
| Project Artifact under change control | Of the project artifacts, which are under change control. |
| Risk Breakdown and management | Identify the project risks and management plan for the risks |
| Project Repository | The project repository structure |
| Eclipse sub-project under which this project falls | Where does the project align with the Eclipse OpenHW sub-project |
| Initial code contribution description | As described in the PL gate |
| Eclipse Foundation Contribution Questionnaire result (for IP due diligence) | Result of IP due diligence on the initial code contribution |

Table 3 Project Plan Typical Elements

#### *Project Close Gate*

The Project Close Gate signifies the completion of the technical deliverables of a project. If a Maintenance Project is required for ongoing support, bug fix, etc., that Maintenance Project is preferably scoped out and presented to TWG at the same time as the Project Close Gate.

### **Technical Milestones for OTP**

The technical milestones which will be tracked and reported to the OpenHW membership are determined as appropriate for each project. The project team sets out the milestones in the project plan, which is agreed at the PPA Gate by the TWG.

#### *Technical Milestones for Design Integrated Circuit IP OpenHW Technical Project (DIP* OTP)

A Design Integrated Circuit IP (DIP) OTP comprises the design and verification of an RTL “IP block”. For example, a RISC-V core would be designed or imported, and OpenHW would verify the IP. The end-result of a DIP OTP would be fully verified RTL code. A typical flow of technical milestones is shown in Figure 2

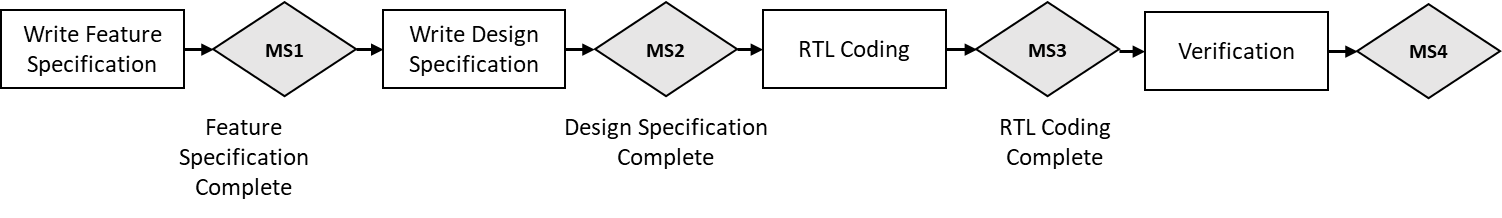


Figure 2 Design Integrated Circuit - Typical Technical Milestones

Typical engineering milestones tracked in OpenHW Integrated Circuit design and verification OTP are shown in Table 4.

|  |  |
| --- | --- |
| **Engineering Milestone** | **Description** |
| Feature and Performance Specification Complete | An agreed Feature and Performance Specification has been reviewed and agreed by the working group. Including external interfaces. AKA Datasheet. |
| Design or Solution Specification Complete | An agreed Design or Solution Specification has been reviewed and agreed by the working group. Internal structure, internal bus specification, etc. Can be optional for existing RTL. |
| User Manual | Define the structure and function of the Control and Status Registers (CSR), interrupts and other aspects used by software integrators will use. |
| RTL Coding Complete | RTL design coding is complete |
| Verification Complete | The Testbench has been reviewed and agreed by the working group, test cases prepared, and test cases run |
| RTL Freeze | Final post-verification RTL coding is complete |

Table 4 Design IP OTP – Typical Technical Milestones

#### Technical Milestones for Verification Integrated Circuit IP Project (VIP OTP)

A variety of Verification Integrated Circuit IP (VIP) projects could be envisaged, for example, a project to develop a RISC-V instruction generator.

Although engineering milestones tracked in a VIP OTP would be highly dependent on the nature of the project, some typical milestones are show in Table 5 . The project team sets out the milestones in the project plan which is agreed at the PPA Gate.

|  |  |
| --- | --- |
| **Engineering Milestone** | **Description** |
| Verification Feature Specification Complete | An agreed Feature Specification has been reviewed and agreed by the working group. |
| Verification Design Specification Complete | An agreed Design Specification has been reviewed and agreed by the working group |
| Verification Design Complete | The Verification tool or capability is completed |

Table 5 Verification IP project - typical milestones

#### Technical Milestones for Software Project (SW OTP)

Software projects may be run according to either waterfall or agile design methodology

**SW Waterfall Approach**

|  |  |
| --- | --- |
| Engineering Milestone | Description |
| Feature Specification Complete | An agreed Feature Specification has been reviewed and agreed by the working group. |
| Design Specification Complete | An agreed Design Specification has been reviewed and agreed by the working group |
| Initial Coding Complete | Initial Coding is complete |
| Testing Complete | Final testing is complete |
| Distribution Complete | Packaging for distribution is complete |

Table 6 - SW OTP - Waterfall Typical Milestones

**SW Agile Approach**

OpenHW Software projects which are run in an agile methodology will need a model which allows initial agreement on a feature specification, then iterative milestones allowing for incremental software releases.

Further investigation is needed to develop the technical milestone tracking strategy for agile projects.

#### Technical Milestones for FPGA Project

Further investigation is needed to develop the technical milestone tracking strategy for FPGA OTP.

#### Technical Milestones for Board Level Hardware Project

Further investigation is needed to develop the technical milestone tracking strategy for Board Level Hardware OTP.

### **Maintenance Projects**

Maintenance Projects are those which will provide ongoing support, bug fix, or minor feature enhancement for projects which reached the Project Close Gate.

They follow a similar Gate Review process for OTP.

|  |  |  |
| --- | --- | --- |
| **Maintenance Project Gate** | **Gate Criteria** | **Activities Leading up to Gate** |
| Maintenance Launch (ML) | * Scope of anticipated ongoing maintenance, bug fix, or minor feature enhancement is identified and approved by TWG * Anticipated duration of maintenance is established * Resource and funding plan is developed and approved by OpenHW CEO | * Scope development for Maintenance Project |
| Maintenance Closed (MC) | * It is established and accepted by TWG that ongoing maintenance activities no longer required * Communication plan for maintenance closure is established, e.g. notification of user community | * Stakeholder discussion to establish that maintenance is no longer needed |

Table 7 - Maintenance Projects - Typical Milestones

## Change Controlled-Artifacts

The OTP Project Plan includes a list of project artifacts and determines which of those artifacts are under change control. For example, an OTP project’s Feature Specification would normally be under change control.

The project plan also specifies related milestones to those change controlled artifacts, such as Feature Description Approved.

A process for modifying a previously approved, change-controlled artifact is required. From a preliminary point of view this process will include:

* The change request can be made by any OpenHW member but would normally be made by an active participant in the OTP.
* A notification to the relevant TG and to the TWG of the request to modify the change-controlled artifact
* A justification for the requested change
* An assessment of schedule and resource impact
* A recommendation by the Project Manager
* An approval or denial by the TWG for the change request

## OpenHW Working Groups

OpenHW working groups are shown at <https://www.openhwgroup.org/working-groups/>

### Technical Working Group (TWG)

The Technical Working Group (TWG) is OpenHW’s permanent, technical supervisory group. The TWG roles are:

* Discussion and planning of overall technical strategy for OpenHW
* Creates and closes Task Groups (TG) as required
* Approves or modifies charters of TG
* Technical roadmap planning, such as discussion of potential (not yet approved) OpenHW projects
* Reviewing new project proposals
* Launching new projects
* Approving Technical Project Leader(s) and Project Manager for OTPs and OSPs
* Reviews project plans for OTPs and OSPs
* Monitoring progress of technical projects carried out by Task Groups (TG).

### Task Groups (TGs)

The Task Groups (TGs) are created and chartered by the TWG. Their charter may be modified by the TWG. TG may be closed by the TWG when no longer needed.

The current TGs and their charters are summarized in the following table:

|  |  |
| --- | --- |
| **OpenHW Task Group** | **Description** |
| Cores Task Group | * Coordinates engineering specification, design and RTL coding effort for OTPs requiring cores related design * Monitors technical milestones of cores design aspects of OTPs * Investigates and decides on engineering tools and methodology related to cores design * Participates in OSPs as required from the cores point of view |
| Verification Task Group | * Coordinates engineering verification efforts for OTPs requiring verification * Monitors technical milestones of verification aspects of OTPs * Investigates and decides on engineering tools and methodology related to verification * Participates in OSPs as required from the verification point of view |
| SW Task Group | * Coordinates software engineering efforts for OTPs requiring software effort * Monitors technical milestones of software aspects of OTPs * Investigates and decides on software engineering tools and methodology * Drives industry outreach on software tools and issues, in conjunction with TWG and staff |
| HW Task Group | * Coordinates software engineering efforts for OTPs requiring FPGA and/or board level design * Monitors technical milestones of hardware aspects of OTPs * Investigates and decides on hardware engineering tools and methodology |

Table 8 - Task Groups

### Working Group Quorum and Voting

Each working group committee in OpenHW, including TWG and TGs, maintains its own quorum and attendance records. These rules are written it the OpenHW Member Agreement <https://www.openhwgroup.org/membership/openhw-group-bylaws-2019-10-16.pdf>. They are summarized below.

#### Quorum

Working groups require 2/3 of their members to be present to form quorum.

#### Voting

Votes in a working group, whether in a meeting or by email ballot, pass by majority vote.

Votes require a quorum of members to be present.

Working group eligible to vote are determined as follows: During the first four (4) meetings of a committee, each Member represented on the working group is eligible to vote on matters brought before the working group. After the first four (4) meetings, each Member represented on the working roup must have had a representative present at three (3) of the four (4) previous working group meetings to be eligible to vote on matters brought before the committee.

### Projects Spanning Several TGs

Some OpenHW projects require the effort of a single Task Group, and some are “vertical” activities which may require effort from several Task Groups.

The table below shows an example of three projects.

The TWG is the central body which reviews project proposals, launches projects, and holds gate reviews.

The TGs carry out the work, hold TG meetings to review issues and coordinate progress, and report technical milestone progress to the TWG.

|  |  |  |  |
| --- | --- | --- | --- |
| Working Group | OpenHW project 1 | OpenHW project 2 | OpenHW project 3 |
| TWG | **** | **** | **** |
| Cores | **** |  |  |
| Verification | **** |  | **** |
| SW |  | **** |  |
| HW |  | **** |  |

Table 9 - Vertical Projects Involving Several TG

### Role of TG Chairs and Project Leader

Project leadership roles are described in Section 1.1.1

The TWG and TGs each have a chair or co-chairs who convene meetings, publish meeting minutes, and act as subject matter leaders in their respective Task Group areas.

The Technical Project Leader/Project Managers work closely together with the chairs or cochairs of the relevant TGs to address and resolve project issues. The TG chairs may themselves act as Technical Project Leaders or Project Managers.

Technical milestones and project issues are normally discussed at TG meetings. Technical Project Leaders or Project Managers explain the status of technical milestones during these meetings. TG level-votes are held to approve technical project milestones.

## Project Visibility on OpenHW Group Website

The current list of OpenHW OTPs and OSPs is available on the OpenHW Group Website at <https://www.openhwgroup.org/projects/>

Note that the current content on this page will be updated with the specific list of OTPs and OSPs,

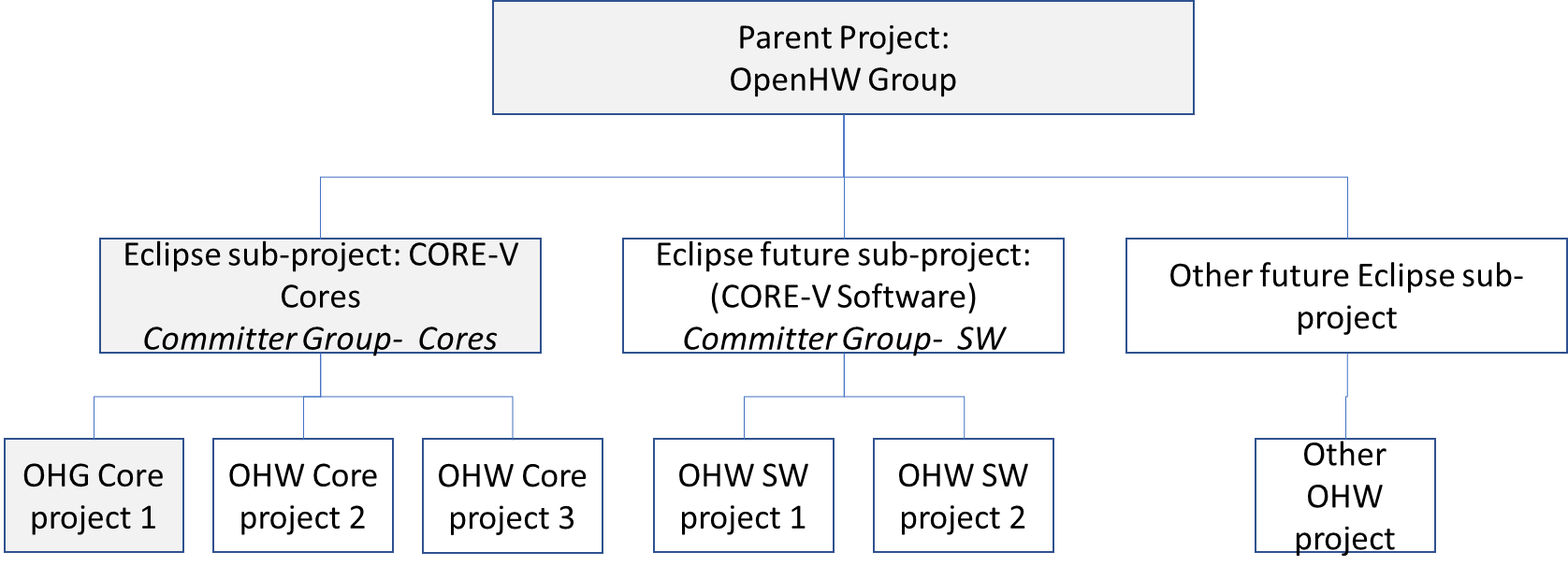
It is to be decided which gate and milestone information is made public.

# **OpenHW Projects from the Eclipse Foundation Perspective**

OpenHW collaborates with the Eclipse Foundation and makes use of the Eclipse Development Process (EDP) for open source projects.

The Eclipse Foundation maintains a hierarchical project structure corresponding to the OpenHW Group projects.

The following Figure shows the current structure (active Eclipse sub-projects and active OpenHW projects are shown in grey shade). In future, other sub-projects may be instantiated.



**Figure 1.** Organization of OpenHW as Eclipse Foundation Projects

Note that each Eclipse sub-project has an associated set of Committers.

Initial Committer selection is at project initiation. Subsequently, project Committers are elected according to merit-based criteria.

## OpenHW Committer Election Process

*How Committer Election is implemented by OpenHW will go here.*

The two Eclipse existing projects are described below:

## Eclipse Parent Project: OpenHW Group

The Eclipse Foundation’s parent-level project for the OpenHW Group is described at <https://projects.eclipse.org/projects/>. The parent level project doesn’t itself comprise deliverables.

## Eclipse Sub-Project: CORE-V Cores

The Eclipse Foundation’s OpenHW Group CORE-V Cores sub-project is described at <https://projects.eclipse.org/projects/openhw.corev>.

### Scope

The scope of this sub-project includes the set of deliverables related to CORE-V cores that OpenHW undertakes as follows:

* Complete documentation: micro-architecture and a user manual.
* Implementation: RTL model and synthesis scripts for both ASIC and FPGA implementations.
* Verification: both dynamic (simulation) and static (formal) verification environments.

Note that this scope comprises several actual OpenHW Technical Projects.

### Committers

The Committers recognized by the Eclipse Foundation for this sub-project are shown at <https://projects.eclipse.org/projects/openhw.corev/who> .The initial committers on the CORE-V Cores sub-project are the OpenHW technical chairs.

# **Project Management Tools**

TBD - Gantt chart and Kanban/Sprint planning description

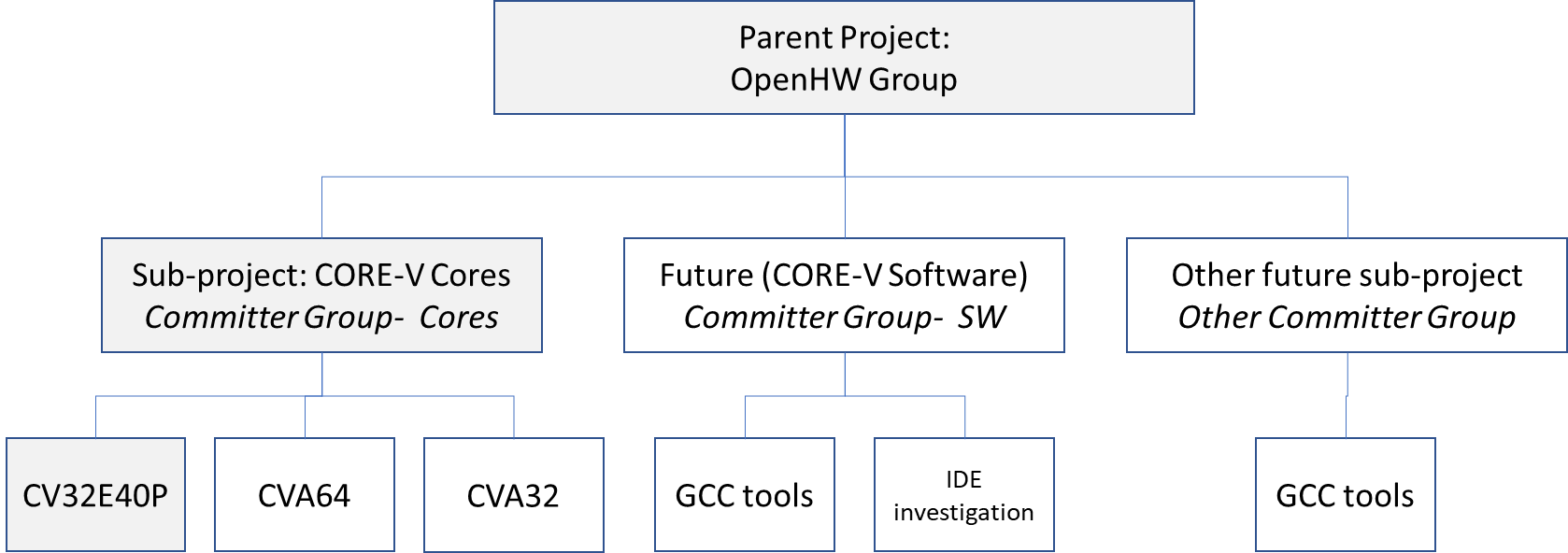
# **Annex 1 – Current OTPs and OSPs**

## Current OTPs and OSPs

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| OpenHW Technical Projects (OTPs) | CV32E40P | CVA64(?) CVA32(?) | GCC SW tools | FORCE-RISCV |
| Description | DIP for a fully verified RTL code for 32-bit embedded processor | DIP for a fully verified RTL code for 32/64-bit application processor | An agreed set of GCC tools (needs full description) | VIP for a RISC-V compliant instruction stream generator |
| Type of Project | OTP | OTP | OTP or OSP, to be decided | OTP |
| TG involved | Cores, Verification, SW | Cores, Verification | SW | VTG |
| Project Leader(s) | Mike Thompson, Davide Schiavone | TBD | Jeremy Bennett | TBD |
| Project Gate passed | **PL** | none | none | none |
| Technical Milestones passed | **list to be created from existing project plans and status updated** |  | none | none |
| Eclipse Sub-Project | CORE-V Cores | CORE-V Cores | potentially CORE-V SW | CORE-V VERIF |

## Current Mapping of OpenHW Technical Projects and Eclipse Sub-Projects

The following Figure shows the current structure (active Eclipse sub-projects and active OpenHW projects are shown in grey shade). In future, other sub-projects may be instantiated.



**Figure 1.** Organization of OpenHW as Eclipse Foundation Projects